IN THE CLAIMS

Please amend the claims as follows:

1. - 19. (Cancelled)

20. (Previously Presented) A method, comprising:

storing one or more prior pop pointer values of a pop pointer;

prior to processing one or more pop requests,

storing data into a memory array of a FIFO memory, and

incrementing a push pointer;

processing one or more pop requests to read data from the FIFO memory;

reading a pop pointer value of the pop pointer and a push pointer value of the push pointer;

determining a status of the memory array in response to the pop pointer value, the push pointer value, a high threshold level, and a low threshold level, where the high threshold level is responsive to the lesser of a maximum branch resolution latency and the low threshold level;

receiving information to indicate at least one of the one or more pop requests was speculative and to indicate that a state of the pop pointer of the FIFO memory should be restored; and

restoring one of the one or more prior pop pointer values to the pop pointer in response to the information.

21. (Previously Presented) The method of claim 20, where,

the maximum branch resolution latency is a depth of an instruction pipeline in a processor, the processor to couple to the FIFO memory.

22. (Previously Presented) The method of claim 20, where,

the information includes a branch resolution latency, the branch latency being the number of instruction cycles to resolve a conditional branch instruction in a processor, the processor to couple to the FIFO memory.

23. - 76. (Cancelled)

77. (New) An apparatus, comprising:

a first storage unit to store one or more prior pop pointer values of a pop pointer;

a FIFO memory;

a push pointer;

a pre-pop request logic that is to store data into a memory array of the FIFO memory and to increment the push pointer prior to processing one or more pop requests;

a pop-request logic to process one or more pop requests to read data from the FIFO memory, to read a pop pointer value of the pop pointer and a push pointer value of the push pointer, to determine a status of the memory array in response to the pop pointer value, the push pointer value, a high threshold level, and a low threshold level, where the high threshold level is responsive to the lesser of a maximum branch resolution latency and the low threshold level;

a receive logic to receive information to indicate at least one of the one or more pop requests was speculative and to indicate that a state of the pop pointer of the FIFO memory should be restored; and

a restore logic to restore one of the one or more prior pop pointer values to the pop pointer in response to the information.

78. (New) The apparatus of claim 77, where,

the maximum branch resolution latency is a depth of an instruction pipeline in a processor, the processor to couple to the FIFO memory.

79. (New) The apparatus of claim 77, where,

the information includes a branch resolution latency, the branch latency being the number of instruction cycles to resolve a conditional branch instruction in a processor, the processor to couple to the FIFO memory.